DC offset leads to saturation of right leg drive output

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ABSTRACT – Due to the high gain that is applied to signal in the right leg drive circuit, the integrity of the RLD signal is easily affected by any direct current (DC) offset present in the RLD circuit. In this report, we have mathematically shown how DC offset affects the RLD output. Then we compared the RLD output with various levels of DC offset. The results show that an offset of 0.1V can saturate the operational amplifier. With a high DC offset, the RLD does not reduce the common mode noise effectively as intended.

1. INTRODUCTION

The RLD circuit is used widely in biosignal acquisition circuits, especially in ECG amplifiers [1-2]. The RLD circuit fundamentally consists of an inverting amplifier.

Typically, the RLD amplifier design has a high gain [3]. Therefore, any DC error margin will be amplified as well. If the common mode signal, V_{cm} and DC offset be V_{dc}, then the resulting V_{RLD} in time domain can be expressed in (1).

$$V_{RLD}(t) = V_{cm}(t + \Delta t_A + \Delta t_C) + V_{dc} \quad (1)$$

In practical op-amps, a small phase lag exists at the output [4]. The phase shift due to the op-amp amplification and capacitance are represented by Δt_A and Δt_C. To function effectively, it the RLD circuit must apply as little phase shift and DC offset as possible. However, the effect of DC offset unto the RLD circuit has not been studied extensively in previous literature.

2. METHODOLOGY

We have identified three sources of DC offset, which are the electrode offset, resistor tolerance and the default DC offset of gain pins of the instrumentation amplifier itself.

As shown in Figure 1, V_{RLD} input voltage, V_G, is taken from the centre tap of the gain resistors R_a and R_b which forms a voltage divider. For the high impedance buffer formed by R_1 and R_2, V_a=V_{in1} and V_b=V_{in2}. Thus theDC output of V_G can be expressed in (2).

$$V_G = V_{in1}\left[\frac{R_a}{R_a+R_b}\right] + V_{in2}\left[\frac{R_b}{R_a+R_b}\right] \quad (2)$$

In an ideal case where R_a=R_b=R, a symmetrical voltage divider is formed, thus

$$V_G = \frac{1}{2}(V_{in1} + V_{in2}). \quad (3)$$

This equation shows that V_G is influenced by the difference between V_{in1} and V_{in2}. By introducing tolerance into R_a and R_b, (3) becomes

$$V_G = \frac{1}{2}(V_{in1} + V_{in2}) - \frac{V_{in1}}{4R}.\Delta R_a + \frac{V_{in2}}{4R}.\Delta R_b. \quad (4)$$

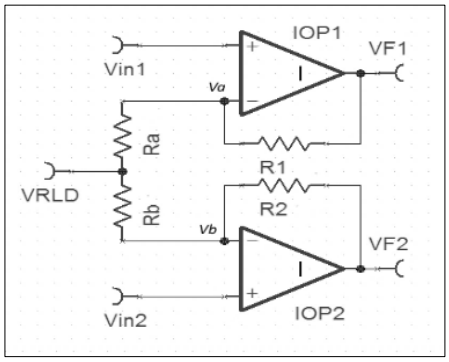

Figure 1 RLD output from instrumentation amplifier.

The deviation of the values $R_a$and$R_a$due to tolerance are represented by $\Delta R_a$and ΔR_a. The experimental setup to demonstrate (2) and (3) is shown in 2.

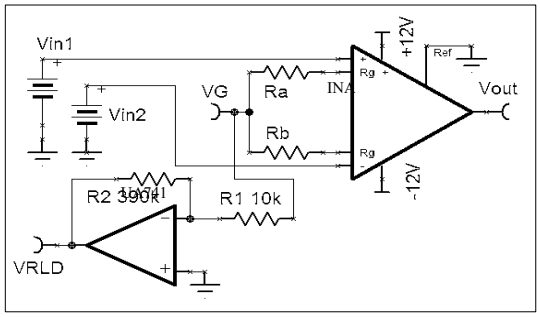

Figure 2 Experimental setup.

The electrode DC offset, represented by V_{in1} and $V_{in2}$are the input. The inverting amplifier with a gain of -39 forms the RLD output. To test the extent of electrode offset difference, V_{in1} and V_{in2}were varied between 0-0.5V. Next, R_a and R_a were varied within 1% and 5% for the tolerance effect. Finally, with V_{in1} and V_{in2} grounded, the integrated amplifier (INA) was measured for DC offset at the VG output.

3. RESULTS AND DISCUSSION

The result of V_G and V_{out} due to input offset is shown in Figure 3. The half-cell potential of the Ag-Cl electrode is rated at 0.223V. However, this voltage can vary by adhesion, pressure and age of the electrode. For V_{out}, the differential amplifier rejects common mode input voltage. Hence V_{out} will trend towards zero when $V_{in1} = V_{in2}$, as shown in Figure 4. Unlike V_{out}, V_G averages V_{in1} and V_{in2}, thus any DC offset will be amplified as in (3) and (4). For a gain of -39, a 0.1 V DC offset will be amplified to -3.9 V. If the supply voltage is ±12 V, V_{RLD} will go into saturation if the DC offset is above 0.3 V.

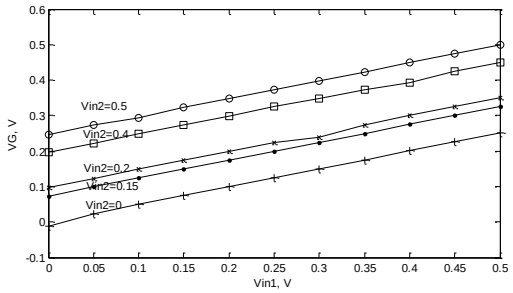

Figure 3 Measured V_G shift due to DC offset at input.

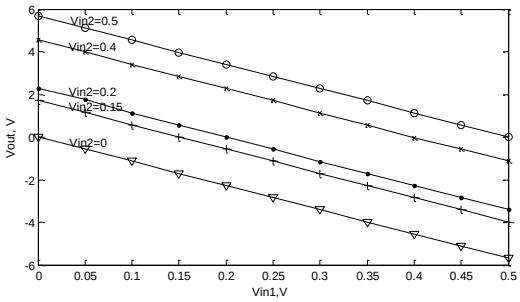

Figure 4 Measured V_{out} shift due to DC offset at input.

In Figure 5, ten pairs of 1 kΩ resistors with 1% and 5% tolerance were randomly selected and the resulting V_G was observed. The deviation of V_G due to resistor tolerance can be minimized to a negligible level by using 1% tolerance resistors. The default offset of INA114 was measured at -0.0014 V, which results an ideal VG of 0.2216 V.

To validate the overall effect of the DC offset at V_G, the electrodes were connected to the flexor digitorum superficialis muscle. An input filter, as suggested in [5] was applied as a fully calibrated setup against a setup with no input filter. The result in Figure 6 shows that a properly calibrated input filter with negligible offset produces a signal with lower floor noise. For the uncalibrated setup, the V_G DC offset was allowed to drive the inverting amplifier to saturation. This reduced the effectiveness of the RLD and a higher floor noise was noticeable.

4. CONCLUSION

Due to the high gain of the RLD output, any DC offset within its signal chain cannot be tolerated. The objective of this study to shown that DC offset can drive the RLD into saturation has been demonstrated. The DC offset due to electrode offset is more detrimental than the imbalance voltage divider of V_G. Therefore, we recommend input filters at the front end and low tolerance resistors for instrumentation gain resistors.

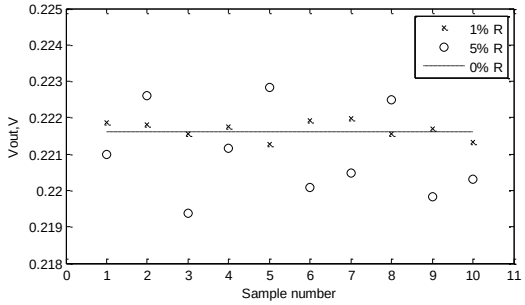

Figure 5 Scatter plot of V_G deviation due to R_a and R_b tolerance.

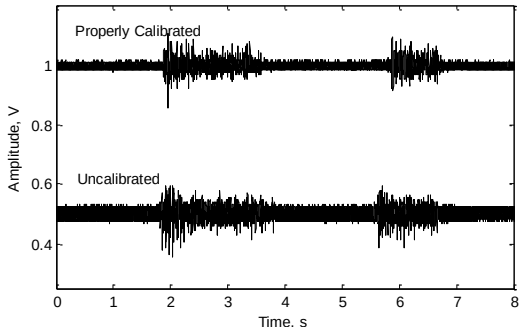

Figure 6 V_{out} with V_G at zero offset (top) vs V_G at saturation (bottom). V_{out} was offset for display purpose.

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