Optimization using L9 Taguchi method toward threshold voltage of 18nm gate length SOI p-channel MOSFET

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ABSTRACT – Silicon on insulator (SOI) technology is proven to effectively counter the short channel effect. In this paper, the characterization of 18nm Gate Length of SOI p-channel MOSFET has been studied according to the latest prediction of the International Technology Roadmap Semiconductor (ITRS). The optimization approach is mainly focused on the threshold voltage (V_{TH}) of device through L_9 Taguchi method. There are four process parameters were varied into three different levels in order to conduct nine set of experiments. At the end of the experiments, the best setting of the process parameters that have been predicted by Taguchi method were used for verification. The result shows V_{TH} after optimization approaches is closer to the nominal value (-0.533V), which is well within the ITRS 2013 specifications.

1. INTRODUCTION

As the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) becomes more minuscule, the number of atoms in the silicon that engender many of the transistor's properties is becoming fewer, with the result that control of dopant numbers and placement is more erratic [1]. The introduction of a method that called Buried oxide thickness deposition has brought the significant impact to the technology of MOSFET. With this improved method which is known as Silicon-on-insulator (SOI) MOSFET, the electrical characteristic of MOSFET can be further improved. This happens due to the advantage of SOI technology that can mitigate the short channel effect (SCE) problem [2].

The SCE is a crucial problem to a MOSFET when the dimension of the device is scaled down. It is assumed that the SOI device have the advantages of speed about 20 to 30 percent more expeditious and consume one-third to one-half the puissance of bulk MOSFET [2]. SCE has become the major threat in conventional MOSFET device structure. SCE occurs when the source and drain region become too proximate to each other. If the effective channel length (L_{eff}) is too short, the depletion region from drain will reach the source region and subsequently reduces the barrier for electron injection. As a result, the electrical characteristic of the device will be degraded.

In this paper, the virtual fabrication of the transistor device is done by utilizing ATHENA module, meanwhile the simulation for electrical examination is done by utilizing ATLAS module from SILVACO software [3]. For identify semiconductor process parameters whose variability would impact most on the device characteristics is realized using Taguchi Method. Taguchi method has become a potent implement for ameliorating productivity during research and development. Through the implementation of Taguchi method, the final product or process can enhance the quality at minimum time and cost [4,5].

2. METHODOLOGY

In this research, there are 3 stages such as designing stage, extraction of electrical characteristic stage and optimization of process parameter stage. For the designing stage Athena module from Silvaco TCAD tools been used while for the extraction stage Atlas module been use to tabulate the result [3]. The L_9 orthogonal array of Taguchi method been used for optimization process. Based on the Table 1, the process parameter and their level has been determined. Four process parameter among other parameters have been chosen.

Table 1 Process parameter and their level

Sym	Process parameter	Unit	Level 1	Level 2	Level 3
A	Halo implant Dose	Atom cm^{-3}	1.72e13	1.73e13	1.74e13
B	Halo Implant Energy	keV	157	158	159
C	S/D Implant Dose	Atom cm^{-3}	2.97e13	2.98e13	2.99e13
D	S/D implant Energy	keV	57	58	59

The four process parameters are halo implant energy, halo implant dose, Source/Drain (S/D) implant dose and S/D implant energy. Among all the process parameters, these four process parameters are parameters which give more impact on electrical characteristic [5]. Table 2 shows the noise factor that will be used in this optimization process parameter using L_9 Orthogonal Array Taguchi method.

Table 2 Noise factor and their level

Symbol	Noise Factor	unit	Level 1	Level 2
M	Sacrificial Oxide Temperature	°C	600	601
N	Annealing Process Temperature	°C	910	912

3. RESULT AND DISCUSSION

Figure 1 shows the S/N ratio (Nominal the best) graph where the dashed line is the value of the total mean of the S/N ratio. In this research, V_{TH} of the device belongs to the nominal-the-best quality characteristics. This S/N Ratio is selected to get closer or equal to a given target value, which is also known as nominal value The total mean for this V_{TH} is 51.25dB. V_{TH} is the main response to determine either the device work or not but the other characteristic also need to be keep as best as possible. Basically the larger the S/N ratio, the quality characteristic of V_{TH} is better [5,6].

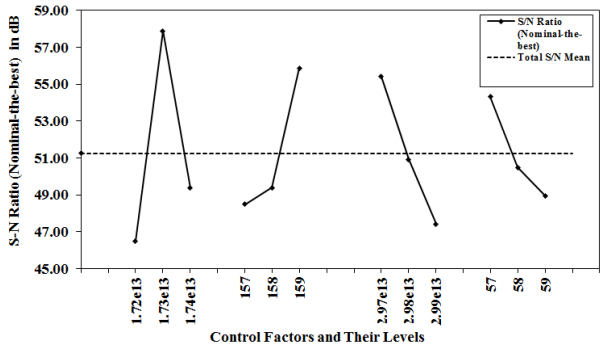

Figure 1 S/N graph of V_{TH} for SOI p-channel device

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The results of analysis of variance (ANOVA) for the 18nm gate length SOI p-channel MOSFET device are shown in Table 3. According to these analyses, the major factor effecting the V_{TH} is halo implant dose (Factor A) with 47% whereas the second ranking factor was halo implant energy (Factor B) that is 22%. Percent factor effect on S/N Ratio indicates the relative power of a factor to reduce variation. For a factor with a high percent contribution, a small variance will have a great influence on the performance [6]. Based on the result of ANOVA, it clearly can be defined that, S/D implant energy (Factor D) as an adjustment factor because it has small effect on the variance (10%) and large effect on the mean (84%).

Table 3 Result of ANOVA for SOI p-channel MOSFET device

Symbol	Degree Freedom	Sum of Square	Mean Square	F-value	Factor Effects on SNR (%)	Factor Effects on Mean (%)
A	2	211	105	23	47[a]	2
B	2	98	49	11	22[a]	14
C	2	97	48	11	21	0
D	2	46	23	5	10	84

[a]At least 95% confidence.

The analysis of average performance showed that optimized levels of the process parameters that has been suggested by Taguchi method is $A_2B_3C_1$. Because Factor D was found as adjustment factor in V_{TH}, it could be set at any level [6]. The full recommendation for optimization is $A_2B_3C_1D_2$. The mean for V_{TH} after optimization approaches is -0.50V. This value is still in range ±12.7% from the nominal (target) value, -0.533V [7]. The value is also closer with ITRS prediction. This shows that Taguchi Method can predict the optimum solution in finding the 18nm gate length SOI p-channel MOSFET device with appropriate threshold voltage value.

4. CONCLUSION

As conclusion, this paper focuses on optimizing the process parameter of threshold voltage. Based on the ANOVA method, halo implant dose was identified as the most impact on the V_{TH} of the 18nm gate length SOI p-channel MOSFET device. Meanwhile, S/D implant energy was identified as an adjustment factor in the device. This adjustment factor has been used to get the value of V_{TH} closer to the target (–0.533V). The percent different of V_{TH} value from the target after the optimization approach are just ±6.19%. This value is within the range and closer with ITRS prediction. It can be shown that the optimum solution in achieving the desired transistor was successfully predicted by using Taguchi Method.

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