Study of electrical characteristic for 50nm and 10nm SOI body thickness in MOSFET device

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ABSTRACT – Silicon on insulator (SOI) technology is an effective approach of mitigating the short channel effect (SCE) problems. The SOI is believed to be capable of suppressing the SCEs, thereby improves the overall electrical characteristics of Metal Oxide Semiconductor Field Effect Transistor (MOSFET) device. SCE in SOI MOSFET are heavily influenced by thin film thickness, thin-film doping density, buried oxide thickness and etc. This paper will analyze the effect of buried oxide layer thickness (BOX) towards SOI MOSFET device. The 50nm and 10nm thickness of buried oxide in SOI MOSFET was developed by using SILVACO TCAD tools. From the observation made, the electrical characteristic of 50nm BOX thickness is slightly better than 10nm. It is observed that the value drive current (I_{ON}) of 10nm BOX thickness SOI MOSFET was only 6.9% lower than 50nm. However, the electrical characteristics of 10nm BOX thickness SOI MOSFET are still in the range of ITRS 2013 prediction.

1. INTRODUCTION

Silicon-on-insulator (SOI) MOSFET development was improves a lot lately with a lot of researcher try to improve this technology with a new approach. Silicon-on-insulator or known as SOI now not limited to single gate but now it will be implanted in double gate and maybe triple gate later. The history of SOI MOSFET can be trace back from 80 year ago when J.E Lilienfield introduced first field effect concept called method and apparatus for controlling electric current. He state on his concept, there are three terminal device where the source to drain current is controlled by a field effect from the gate and is dielectrically insulated from the rest of the device. The active part of the device was built on a thin semiconductor film which is deposited on an insulator, believe or not this first proposed FET concept was indeed an introduction of SOI MOSFET, But due to lack of equipment and technologies, this concept been long forgotten until the development of SIMOX or known as implanted oxygen technology in 1966. The main route for this silicon on insulator technology is using silicon dioxide (SiO2) as main material.

Short channel effect (SCE) was the main problem for MOSFET when it comes to scaling down to become Ultra-thin Body (UT). SCE happen, when the barrier of electron injection accidently been reduce due to the effective channel length (L_{eff}) becoming too short. This SCE can lead to several problems to MOSFET model such as a shift of Threshold voltage when channel length been decrease, lack of pinch off. Furthermore, SCE shows that it reduced the controllability of gate voltage and drain current thus increasing drain-off current and degradation of subthrehold slope. Thus SOI MOSFET been introduce to reduced short channel effect (SCE) influenced, although this SOI MOSFET still having short channel effect (SCE) but it still btter then conventional bulk MOSFET. Most of SCE from SOI MOSFET was influenced from thin film thickness, thin-film doping density, substrate biasing and buried oxide thickness. This research is about the effect of electrical characteristic of SOI MOSFET when the buried oxide thickness been varied

2. METHODOLOGY

Initially, P-type silicon with <100> orientation was developed. Then, the Buried Oxide Layer (BOX) formation was created. After that, 200Å oxide layer was grown on top of silicon bulk. This oxide layer had been used as mask during P-well implantation process. After doping process completed, the oxide layer been etched and it was followed by annealing process. This annealing process been done to strengthen the structure. After that process, shallow trench isolation (STI) has been conducted to isolated neighbour transistor. A 130Å stress buffer been applied on the wafers with 25 min diffusion processes. LPCVD process or known as Low-Pressure Chemical Vapour Deposition been used to deposited a 1350Å nitride layer. The purpose of this nitride was to act as mask when silicon was etched to expose the STI area. Photo resistor layer then deposited on the wafer layer and unwanted part will be etched using the Reactive Ion Etching (RIE) process. Purpose for Oxide layer been grown on the trench sides is to eliminate impurity from entering the silicon substrate.

After that, to eliminate extra oxide on the wafer, the chemical Mechanical polishing (CMP) was applied and final process the STI was annealed for 15 minute at 900°C temperature. A sacrificial oxide layer was then grown and etched to eliminate any defect that occur on the surface, before Boron Difluoride (BF2) threshold-adjustment been done in the channel region the gate

oxide must be grown first. The polysilicon gate was then deposited and followed by halo implantation. Indium was doped to get a better performance for every MOSFET. Depositing sidewall spacer then been conducted and been used as mask for source/drain implantation. Arsenic was implanted with certain value of concentration to get smooth current flow in NMOS device, after that silicice layer been produced and then be annealing at the top of polysilicon.

After all the process, the next stage is to deposited Boron Phospor Silicate Glass (BPPG) layer. This layer will acted as Premetal dielectric (PMD) that will be the first layer deposited in the wafer surface when transistor produced. This transistor then will be connected with aluminum metal, after that second aluminum layer was deposited on top of the intel-Metal Dielectric (IMD) and unwanted aluminum was etched to create the contacts. The step was ended when etching and metallization was performed for electrode formation and bonding pad was opened.

3. RESULTS AND DISCUSSION

Figure 1 shows the overlay graph Gate Voltage (V_G) versus Drain Current (I_D). It shown clearly that the value of I_{ON} for 50nm and 10nm SOI MOSFET is 707.48µA/µm and 658.29µA/µm respectively. For I_{OFF} value, the different between 50nm and 10nm are also not having any major different and both are still in value of ITRS 2013. Based on the analysis, it can be seen that both of them have a good transition between off and on states.

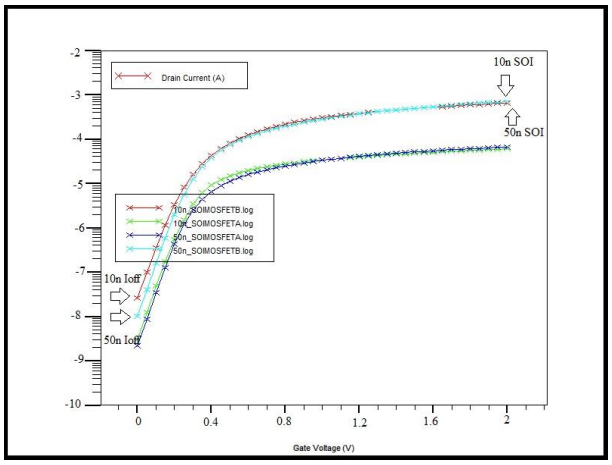

Figure 1 Overlay of 10nm and 50nm I_{ON} and I_{OFF} value.

Table 1 shows specifically the value of 4 electrical value that been measured for both 10nm and 50nm SOI MOSFET device.

Table 1 Electrical Characteristic of 50nm and 10nm SOI MOSFET

Electrical characteristic	**50nm**	**10nm**
I_{ON} (µA/µm)	707.48	658.289
I_{OFF} (pA/µm)	10.64	25.86
S_S (mV/dec)	82.96	85.59
V_{TH} (V)	0.2887	0.2896

4. CONCLUSIONS

This paper focus on study of electrical characteristic of SOI MOSFET when thickness of Buried Oxide layer been modified and then those value been compared to ITRS 2011 value either it still on range of ITRS value or not. The analysis of result shows that the value of 50nm and 10nm SOI MOSFET. It shown that the value of I_{ON} for 10nm SOI MOSFET device is 6.9% slightly lower than 50nm. However this value is still applicable in ITRS 2013.

5. REFERENCES

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