Taguchi modeling of process parameters in VDG-MOSFET device for higher I_{ON}/I_{OFF} ratio

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ABSTRACT – The miniaturization in the size of planar MOSFET device seems to be limited when it reaches to 22nm technology node. The most common approach to overcome this problem is to replace silicon dioxide (SiO_2) and polysilicon with high-k dielectric material and metal gate respectively. However, in this paper, the vertical double gate architecture of MOSFET device with ultrathin pillar was introduced by keeping both silicon dioxide (SiO_2) and polysilicon as the main materials. The proposed MOSFET architecture was known as Ultrathin Pillar Vertical Double Gate (VDG) MOSFET device and it was integrated with polysilicon-on-insulator (POI) technology for a superior electrical performance. The virtual device's fabrication and characterization were done by using ATHENA and ATLAS modules of SILVACO Internationals. The process parameters of the device were then optimized by utilizing L_{27} orthogonal array of Taguchi method in order to obtain the highest value of drive current (I_{ON}) and the lowest value of leakage current (I_{OFF}). The highest value of I_{ON}/I_{OFF} ratio was observed to be 2.154×10^{12}. Whereas the nominal threshold voltage (V_{TH}), drive current (I_{ON}), leakage current (I_{OFF}) and sub-threshold swing (SS) were observed to be 0.437 V (±12.7% of 0.447 V), 701.9 µA/µm, 9.374×10^{16} A/µm and 63.66 mV/dec respectively. These results are well within the prediction value of International Technology Roadmap Semiconductor (ITRS) 2013 for low power (LP) multi-gate (MG) technology requirement in year 2020.

1. INTRODUCTION

Producing planar MOSFET devices with a very short channel length seems to be very challenging and complicated especially for below 22nm technology node. The reduction of MOSFET's size is always related to the deterioration of the device's characteristics. The most critical device's characteristics that are important to be preserved are known as drive current (I_{ON}) and leakage current (I_{OFF}). An attempt to reduce the physical gate (Lg) of conventional MOSFET device has result in a very close proximity between drain region and the source region thereby introducing various short channel effect (SCE) problems. These SCEs lead to the increase of leakage current (I_{OFF}) which will deteriorate the device's performance. A lot of researches have been done to circumvent these SCE problems. One of them is to integrate the combination of high permittivity (high-k) dielectric material and metal gate into the MOSFET's structure. However, in this current research, traditional silicon dioxide (SiO_2) and polysilicon material are still being used by introducing ultrathin pillar polysilicon-on-insulator (POI) Vertical Double Gate (VDG) design architecture.

This paper emphasizes on utilizing L_{27} orthogonal array of Taguchi method that consists of thirteen process parameters which are substrate implant dose, V_{TH} implant dose, V_{TH} implant energy, halo implant energy, halo implant tilt, source/drain (S/D) implant dose, compensation implant dose and etc. The gate oxide temperature and polysilicon oxidation temperature are selected as noise factors in order to get the optimum results. The main objective of the current work is to maximize the drive current (I_{ON}) value and to minimize the leakage current (I_{OFF}) value. Besides that, the threshold voltage (V_{TH}) value must be ensured to be within ±12.7% of low power (LP) multi-gate (MG) requirement in ITRS 2013 prediction (0.447V) for year 2020.

2. MATERIALS AND METHODS

2.1 Virtual Fabrication Process

The virtual fabrication process of VDG-MOSFET device was simulated by using ATHENA and ATLAS modules of SILVACO International. ATHENA module was used for process simulation of MOSFET's device. Meanwhile, ATLAS module was used for device simulation and electrical characterization.

Compensation implantation was utilized later by implanting phosphor dosage of 2.51×10^{12} atom/cm^3 with energy level of 63 Kev and tilt angle of 7°. This step is taken in order to reduce parasitic effects that could increase the leakage current (I_{OFF}). Next, silicide (CoSi) was formed on the source and drain region by sputtering cobalt on silicon surface. This transistor was then connected with aluminum metal. The aluminum layer was deposited on the top of the Intel-Metal Dielectric (IMD) and unwanted aluminum was etched to develop the contacts [1]. The procedure was completed after the metallization and etching were performed for the electrode formation, and the bonding pads were opened. The final structure of VDG-MOSFET device

was completed by mirroring the right-hand side structure. The completed structure of VDG-MOSFET device is illustrated as in Figure 1.

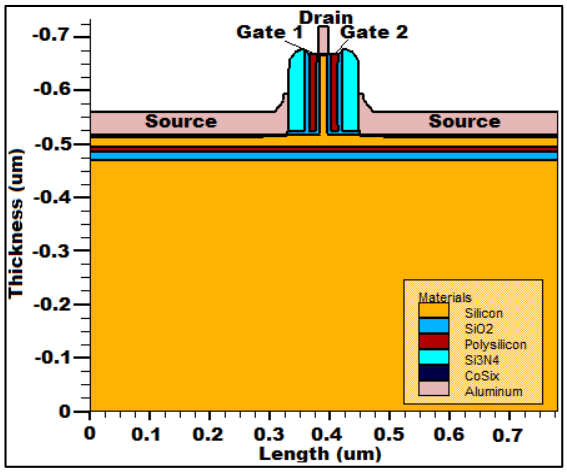

Figure 1 Structure of VDG-MOSFET device

Table 1 L_{27} Orthogonal Array Taguchi Method

Exp No.	Process Parameter Level												
	A	B	C	D	E	F	G	H	J	K	L	M	N
1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	1	1	1	1	2	2	2	2	2	2	2	2	2
3	1	1	1	1	3	3	3	3	3	3	3	3	3
4	1	2	2	2	1	1	1	2	2	2	3	3	3
5	1	2	2	2	2	2	2	3	3	3	1	1	1
6	1	2	2	2	3	3	3	1	1	1	2	2	2
7	1	3	3	3	1	1	1	3	3	3	2	2	2
8	1	3	3	3	2	2	2	1	1	1	3	3	3
9	1	3	3	3	3	3	3	2	2	2	1	1	1
10	2	1	2	3	1	2	3	1	2	3	1	2	3
11	2	1	2	3	2	3	1	2	3	1	2	3	1
12	2	1	2	3	3	1	2	3	1	2	3	1	2
13	2	2	3	1	1	2	3	2	3	1	3	1	2
14	2	2	3	1	2	3	1	3	1	2	1	2	3
15	2	2	3	1	3	1	2	1	2	3	2	3	1
16	2	3	1	2	1	2	3	3	1	2	2	3	1
17	2	3	1	2	2	3	1	1	2	3	3	1	2
18	2	3	1	2	3	1	2	2	3	1	1	2	3
19	3	1	3	2	1	3	2	1	3	2	1	3	2
20	3	1	3	2	2	1	3	2	1	3	2	1	3
21	3	1	3	2	3	2	1	3	2	1	3	2	1
22	3	2	1	3	1	3	2	2	1	3	3	2	1
23	3	2	1	3	2	1	3	3	2	1	1	3	2
24	3	2	1	3	3	2	1	1	3	2	2	1	3
25	3	3	2	1	1	3	2	3	2	1	2	1	3
26	3	3	2	1	2	1	3	1	3	2	3	2	1
27	3	3	2	1	3	2	1	2	1	3	1	3	2

2.2 Taguchi L_{27} Orthogonal Array Method

In the current research, Taguchi L_{27} orthogonal array is developed in order to investigate the impact of thirteen process parameters on I_{ON}/I_{OFF} ratio. The design of experiment (DoE) consists of 27 experiment rows with different combination level of process parameters is constructed as shown in Table I.

3. RESULTS AND DISCUSSION

From Figure 2, it was observed that factor A1, B1, C2, D3, E1, F1, G3, H2, J3, K1, L3, M1 and N1 have been selected as the optimum value for drive current (I_{ON}) due to their highest SNR. Meanwhile, Figure 3 indicates that factor A2, B2, C1, D1, E3, F1, G1, H3, J2, K1, L1, M3 and N3 were the most optimum value for leakage current (I_{OFF}).

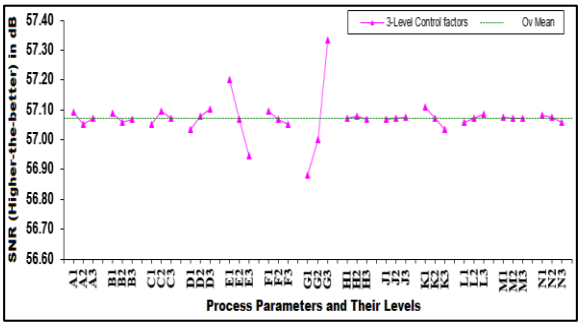

Figure 2 Factor effect plot for SNR (Higher-the-better) for Drive Current (I_{ON})

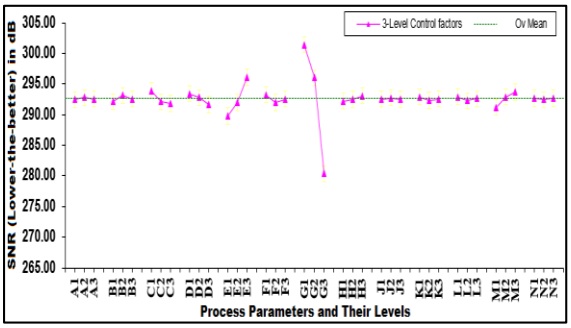

Figure 3 Factor effect plot for SNR (Lower-the-better) for Leakage Current (I_{OFF})

4. REFERENCES

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